TMC22290

Multistandard Digital Video Encoder

Features

- All-digital video encoding
- Internal digital subcarrier synthesizer
- 8-bit parallel CCIR-601/CCIR-656/ANSI/SMPTE 125M input iormat
- CCIR-624/SMPTE-170M compliant output
- Switchable chrominance bandwidth
- Switchable pedestal with gain compensation
- Pre-programmed horizontal and vertical timing
- 13.5 Mpps pixel rate
- Synchronizes to incoming data stream
- Subcarrier phase and frequency values may be input through ancillary data packet in video stream
- Internal interpolation filters simplify output reconstruction filters
- 9-bit D/A converters for video reconstruction
- Supports NTSC and PAL standards
- Output encoding per Macrovision copy protection (Revision 6) available (TMC22291)
- Simultaneous S-Video (Y/C) output
- Controlled edge rates
- TAG (IEEE Std 1149.1-1990) test interface
- Single +5V power supply
- 44 lead PLCC package
- Parallel and serial control interface

Applications

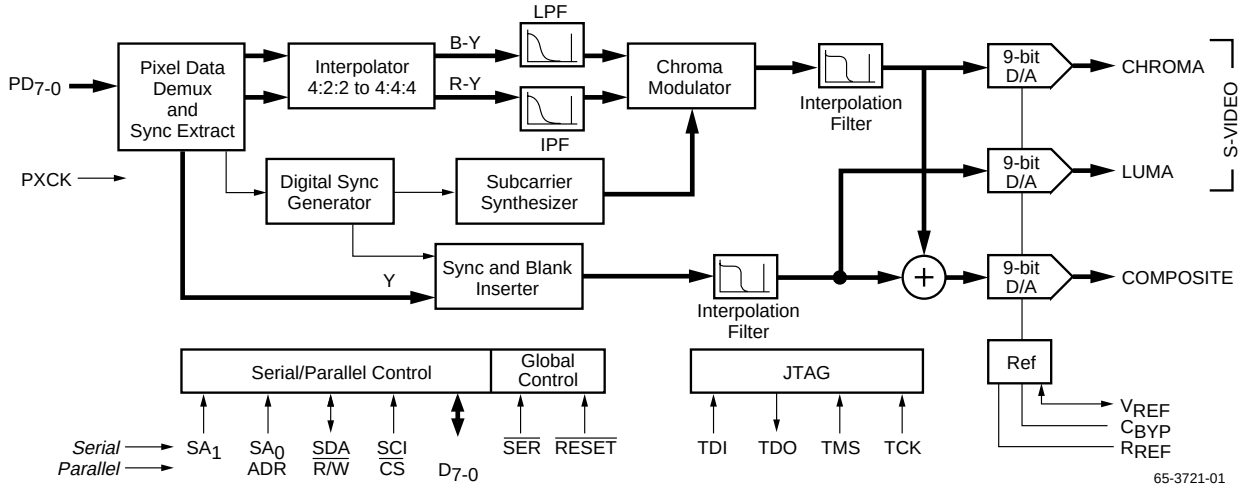
- Settop Digital Cable Television Receivers
- Settop Digital Satellite Television Receivers
- Studio Parallel CCIR-601 to Analog Conversion

Description

The TMC22290 video encoder converts digital component video (in 8-bit parallel CCIR-601/656 or ANSI/SMPTE 125M format) into a standard analog baseband television (NTSC, NTSC-EIA, all PAL standards) signal with a modulated color subcarrier. Both composite (single lead) and S-Video (separate chroma and luma) formats are active simultaneously at the three analog outputs. Each video output generates a standard video-level signal capable of driving a singly- or doubly-terminated 75 Ohm load.

The TMC22290 is fabricated in a submicron CMOS process and is packaged in a 44-lead PLCC. Performance is guaranteed over the full 0°C to 70°C operating temperature range.

Block Diagram



Rev. 1.0.0

General Description

The TMC22290 is a fully-integrated digital video encoder with simultaneous composite and Y/C (S-Video) outputs. The TMC22290 video outputs are compatible with NTSC, NTSC-EIA, and all PAL television standards. No external component selection or tuning is required.

To prevent unauthorized video taping, the output data stream may be modified per the Macrovision copy protection system (Revision 6). This feature is available on the TMC22291 only to Macrovision licensees. Consult the factory for information.

The encoder accepts digital component video at the PD port in 8-bit parallel CCIR-601/656 format. It is demultiplexed into luminance and chrominance components. The chrominance components modulate a digitally synthesized subcarrier. The luminance and chrominance signals are separately interpolated to twice the input pixel rate and converted to analog levels by 9-bit D/A converters. They are also digitally combined and the resulting composite signal is output by a third 9-bit D/A converter.

The encoder operates from a single clock of 27 MHz, twice the system pixel rate. Programmable control registers allow the software control of subcarrier frequency and phase parameters. Incoming YC_BC_R422 digital video is interpolated to YC_BC_R444 format for encoding.

Internal control registers can be accessed over a standard 8-bit parallel microprocessor port or a 2-pin (clock and data) serial port.

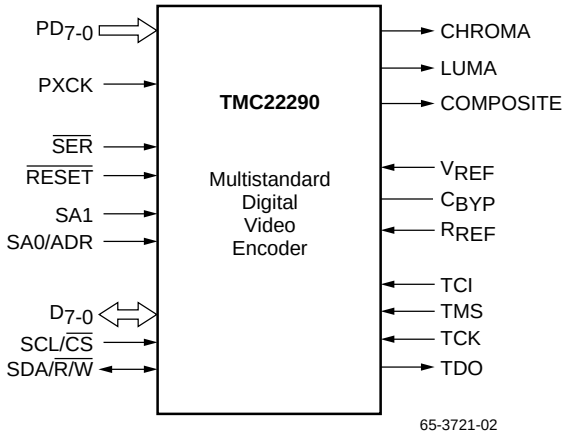


Figure 1. Logic Symbol

MSB						LSB
PD_7			C_B (n)			PD_0
PD_7			Y (n)			PD_0
PD_7			C_R (n)			PD_0
PD_7			Y (n+1)			PD_0

Samples C_B(n), Y(n), and C_R(n) are cosited.

Figure 2. Pixel Data Format

Sync Generator

The TMC22290 operates in a slave mode, extracting its horizontal and vertical sync timing and field information from the CCIR-656 EAV (End of Active Video) signal in the incoming data stream.

Horizontal and vertical synchronization pulses in the analog output are digitally generated by the TMC22290 with controlled rise and fall times on all sync edges, the beginning and end of active video, and the burst envelope.

Chroma Modulator

A digital subcarrier synthesizer drives a quadrature modulator, producing a digital chrominance signal. The chroma bandwidth may be programmed to 650kHz or 1.3 MHz. The relative phases of the burst and active video portions of the subcarrier can be adjusted with respect to the falling edge of horizontal sync. This sets the SCH phasing of the TMC22290. SCH phase adjustment can be accomplished through the parallel or serial ports as well as the ancillary data prior to each line of incoming video.

Interpolation Filters

Interpolation filters on the luminance and chrominance signals double the pixel rate in preparation for D/A conversion. This low-pass filtering and oversampling process greatly simplifies the output filter required after the D/A converters and dramatically reduces sin(x)/x distortion.

D/A Converters

The analog outputs of the TMC22290 are driven by three 9-bit D/A converters, operating at 27 MHz. The outputs drive standard video levels into 37 or 75 Ohm loads. An internal voltage reference is used to provide reference current for the D/A converters. For more accurate video levels, an external fixed or variable voltage reference source is accommodated. The video signal levels from the TMC22290 may be adjusted to overcome the insertion loss of analog low-pass output filters by varying R_{REF} or V_{REF}.

Parallel and Serial Microprocessor Interfaces

The parallel microprocessor interface employs 14 pins. These are shared with the serial interface, and a single pin, $\overline{SER}$, selects between the two interface modes.

In parallel interface mode, one address line is decoded for access to the internal control register and its pointer. Controls are reached by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data (read or write) for that address. The control register address pointer auto-increments to address 20h and then remains there.

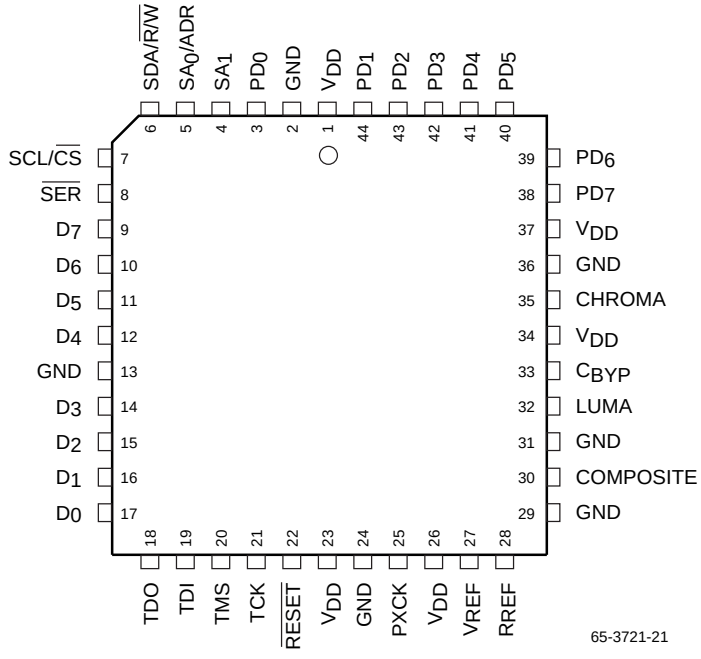
A 2-line serial interface is also provided on the TMC22290 for initialization and control. The same set of registers accessed by the parallel port is available to the serial port.

The $\overline{\text{RESET}}$ pin sets all internal state machines to their initialized conditions, disables the analog outputs, and places the encoder in a power-down mode. All register data are maintained while in power-down mode. At power-up. the encoder is automatically initialized in NTSC-M format.

JTAG Test Interface

The TMC22290 includes a standard 4-line JTAG (IEEE Std 1149.1-1990) test interface port, providing access to all digital input/output data pins. This is provided to facilitate component and board-level testing.

Pin Assignments



Pin Descriptions

Name	Pin Number	Value	Pin Function Description
Clock			
PXCK	25	TTL	**Pixel Clock Input.** This 27.0 MHz clock is internally divided by 2 to generate the internal pixel clock. PXCK drives the entire TMC22290, except the asynchronous microprocessor interface. All internal registers are strobed on the rising edge of PXCK.
Data Input			
PD_{7-0}	38-44, 3	TTL	**Pixel Data Inputs.** Video data enter the TMC22290 on PD_{7-0} (Figure 2).
µProc I/O			
$\overline{\text{RESET}}$	22	TTL	**Master Reset Input.** Bringing $\overline{\text{RESET}}$ LOW forces the internal state machines to their starting states, sets all control registers to their default values, and disables all outputs.
D_{7-0}	9-12, 14-17	TTL	**Data I/O Port.** Parallel control port. When $\overline{\text{SER}}$ is HIGH, all control parameters are loaded into and read back over this 8-bit port. When $\overline{\text{SER}}$ = LOW, D_0 serves as a composite sync output, D_1 outputs a burst flag during the back porch, D_{2-5} are General Purpose Outputs, and D_{6-7} are General Purpose Inputs.
SA_1	4	TTL	**Serial Address Select.** When $\overline{\text{SER}}$ is LOW, SA_1 in conjunction with SA_0 selects one-of-four addresses for the TMC22290.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
$\overline{SER}$	8	TTL	**Serial/Parallel Port Select.** When LOW, the 2-line serial interface is activated. Pins 5, 6, and 7 function as SA_0, SDA, and SCL respectively. When HIGH, the parallel interface port is active and pins 5, 6, and 7 function as ADR, $\overline{R/W}$, and $\overline{CS}$ respectively.
SA0/ADR	5	TTL	**Serial/Parallel Port Address.** When $\overline{SER}$ is LOW, SA_0 in conjunction with SA_1 selects one-of-four addresses for the TMC22290. When $\overline{SER}$ is HIGH, this control governs whether the parallel microprocessor interface selects a table address or reads/writes table contents. It also governs setting and verification of the TMC22290's internal operating modes, also over port D_{7-0}.
SDA/$\overline{R/W}$	6	R-Bus/TTL	**Serial Data/Read/Write Control.** When $\overline{SER}$ is LOW, SDA is the data line of the serial interface. When $\overline{SER}$ is HIGH, the pin is the read/write control for the parallel interface. When $\overline{R/W}$ and $\overline{CS}$ are LOW, the microprocessor can write to the control registers over D_{7-0}. When $\overline{R/W}$ is HIGH and $\overline{CS}$ is LOW, it can read the contents of any selected control register over D_{7-0}.
SCL/$\overline{CS}$	7	R-Bus/TTL	**Serial Clock/Chip Select.** When $\overline{SER}$ is LOW, SCL is the clock line of the serial interface. When $\overline{SER}$ is HIGH, the pin is the chip select control for the parallel interface. When $\overline{CS}$ is HIGH, the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write parameters over D_{7-0}.
Analog Outputs			
COMPOSITE	30	1.35 V P-P	**Composite NTSC/PAL Video.** Analog output of composite D/A converter, nominally 1.35 volt peak-to-peak into a doubly terminated 75 Ohm load.
LUMA	32	1.35 V P-P	**Luminance-only Video.** Analog output of luminance D/A converter, nominally 1.35 volt peak-to-peak into a doubly terminated 75 Ohm load.
CHROMA	35	1.35 V P-P	**Chrominance-only Video.** Analog output of chrominance D/A converter, nominally 1.35 volt peak-to-peak into a doubly terminated 75 Ohm load.
Reference			
V_{REF}	27	+1.23 V	**Voltage Reference Input.** External voltage reference input, internal voltage reference output, nominally 1.235 V.
C_{BYP}	33	0.1 μF	**Reference Bypass Capacitor.** Connection point for 0.1 mF decoupling capacitor.
R_{REF}	28	787W	**Current-setting Resistor.** Connection point for external current-setting resistor for D/A converters. The resistor is connected between R_{REF} and GND. Output video levels are inversely proportional to the value of R_{REF}.
JTAG I/O			
TDI	19	TTL	**Data Input Port.** Boundary scan data input port.
TMS	20	TTL	**Scan Select Input.** Boundary scan (HIGH) / normal operation (LOW) selector.
TCK	21	TTL	**Scan Clock Input.** Boundary scan clock.
TDO	18	TTL	**Data Output Port.** Boundary scan data output port.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Power			
V_{DD}	1, 23, 26, 34, 37	+5 V	**Power Supply.** Positive power supply circuits.
GND	2, 13, 24, 29, 31, 36	0.0 V	**Ground.** Ground for analog circuits, 0 V.

Control Registers

The TMC22290 is initialized and controlled by a set of registers which determine the operating modes.

An external controller is employed to write and read the Control Registers through either the 8-bit parallel or 2-line serial interface port. The parallel port, D_{7-0}, is governed by pins $\overline{CS}$, $\overline{R/W}$, and ADR. The serial port is controlled by SDA and SCL.

Table 2. Control Register Map

Reg	Bit	Name	Function
TMC22290 Identification Registers			
00	7-0	PARTID2	(Read only = $7F_h$)
01	7-0	PARTID1	(Read only = $3A_h$)
02	7-0	PARTID0	(Read only = 95_h)
03	7-0	REVID	(Read only = Revision #)
Global Control Register			
04	7-6	reserved	
04	5	YCDELAY	Luma to chroma delay
04	4	RAMPEN	Modulated ramp enable
04	3	YCDIS	LUMA, CHROMA disable
04	2	COMPDIS	COMPOSITE disable
04	1-0	FORMAT	Television standard select
Video Output Control Register			
05	7	reserved	
05	6	$\overline{BURSTF}$	Burst flag disable
05	5	CHRBW	Chroma bandwidth select
05	4	SYNCDIS	Sync pulse disable
05	3	BURDIS	Color burst disable
05	2	LUMDIS	Luminance disable
05	1	CHRDIS	Chrominance disable
05	0	PEDEN	Pedestal enable
Horizontal Ancillary Data Control Register			
06	7-6	reserved	
06	5-3	FIELD	Field ID (Read only)
06	2	ANCFREN	Ancillary FREQ enable
06	1	ANCPHEN	Ancillary SCHPH enable
06	0	ANCTREN	Ancillary timing ref. enable
Ancillary Data ID Register			
07	7-0	ANCID	Ancillary identification
Subcarrier Frequency Register			
08	7-0	FREQ3	Subcarrier frequency MSB
09	7-0	FREQ2	Subcarrier freq. 2nd byte
0A	7-0	FREQ1	Subcarrier freq. 3rd byte
0B	7-0	FREQ0	Subcarrier frequency LSB
Subcarrier Phase Offset Register			
0C	7-0	SCHPHM	Subcarrier phase MSBs
0D	7-0	SCHPHL	Subcarrier phase LSBs
General Purpose Port (when $\overline{SER}$=LOW)			
0E	7	PORT7-6	General Purpose Inputs
0E	6	PORT5-2	General Purpose Outputs
0E	1	BURSTF	Burst Flag Output
0E	0	CSYNC	Composite Sync Output
Reserved Registers			
0F-FF	7-0	reserved	

Notes:

1. Functions are listed in the order of reading and writing.
2. For each register listed above, all bits not specified are reserved and should be set to zero to ensure proper operation.

Table 3. Power-Up Default Register Values

Reg	Dflt	Reg	Dflt	Reg	Dflt	Reg	Dflt
00	7F	04	00	08	43	0C	00
01	3A	05	00	09	E0	0D	00
02	95	06	00	0A	F8	0E	xx
03	xx	07	00	0B	3E		

Control Register Definitions

TMC22290 Identification Registers (read only)

Reg	Bit	Name	Description
00	7-0	PARTID2	Reads back $7F_h$
01	7-0	PARTID1	Reads back $3A_h$
02	7-0	PARTID0	Reads back 95_h
03	7-0	REVID	Reads back a value corresponding to the revision letter of the silicon.

Global Control Register (04)

7	6	5	4	3	2	1	0
Reserved		YCDELAY	RAMPEN	YCDIS	COMPDIS	FORMAT	

Reg	Bit	Name	Description
04	7-6		Reserved.
04	5	YCDELAY	When HIGH, the luminance path within the TMC22290 is delayed by one PXCK period. The delay applies only to the LUMA output and may be used to compensate for group delay variation of external filters. When LOW, luminance and chrominance have the same latency. The COMPOSITE output always has equal luminance and chrominance latencies.
04	4	RAMPEN	When HIGH, the TMC22290 outputs a modulated ramp test signal. When LOW, incoming digital video is encoded.
04	3	YCDIS	When HIGH, the LUMA and CHROMA outputs are disabled, reducing power consumption. Set LOW for normal enabled operation.
04	2	COMPDIS	When HIGH, the COMPOSITE output is disabled. Set LOW for normal enabled operation.
04	1-0	FORMAT	Output video format select. Subcarrier frequency, pedestal level, and chrominance bandwidth are independently programmed. 0 0 NTSC 0 1 PAL-B,G,H,I,N 1 0 PAL-M 1 1 Reserved

Control Register Definitions (continued)

VIdeo Output Control Register (05)

7	6	5	4	3	2	1	0
Reserved		$\overline{\text{BURSTF}}$	CHRBW	SYNCDIS	BURDIS	CHRDIS	PEDEN

Reg	Bit	Name	Description
05	7		Reserved.
05	6	$\overline{\text{BURSTF}}$	When $\overline{\text{BURSTF}}$ is LOW, a clamp gate signal is produced on the D1 output and register 0E bit 1
05	5	CHRBW	When LOW, the chrominance bandwidth is ±650 kHz. When HIGH, the chrominance bandwidth is ±1.3 MHz.
05	4	SYNCDIS	When HIGH, horizontal and vertical sync pulses on the COMPOSITE video output are suppressed (blanking level). Color burst, active video, and the COMPSYNC output remain active. Set LOW for normal composite video operation.
05	3	BURDIS	When HIGH, color burst is suppressed (blanking level). Set LOW for normal operation.
05	2	LUMDIS	When HIGH, incoming Y values are forced to the black level. Color burst, CHROMA, and sync are not affected. Set LOW for normal operation.
05	1	CHRDIS	When HIGH, incoming color components CB and CR are suppressed enabling monochrome operation. Output color burst is not affected. Set LOW for normal color operation.
05	0	PEDEN	When LOW, black and blanking are the same level for ALL lines. When HIGH, a 7.5 IRE pedestal is inserted into the output video for NTSC and PAL-M lines 23-262 and 286-525 only. Chrominance and luminance gain factors are adjusted appropriately. PEDEN is valid for NTSC and PAL-M only and should be LOW for all other formats.

Horizontal Ancillary Data Control Register (06)

7	6	5	4	3	2	1	0
Reserved		FIELD			ANCFREN	ANCPHEN	ANCTREN

Reg	Bit	Name	Description
06	7-6		Reserved.
06	5-3	FIELD	Digital field identification. A read-only value of 000 corresponds to field 1 and 111 corresponds to field 8.
06	2	ANCFREN	When HIGH, the TMC22290 gets subcarrier frequency data (FREQ3-0) from incoming ancillary data (in accordance with FRV bit). When LOW, FREQ3-0 registers contain the subcarrier frequency data.
06	1	ANCPHEN	When HIGH, the TMC22290 gets subcarrier phase offset data (SCHPHL and SCHPHM) from incoming ancillary data (in accordance with PHV bit). When LOW, a default value of 0000h is used for subcarrier phase.
06	0	ANCTREN	When HIGH, the TMC22290 decodes incoming ancillary data to determine video timing (FIELD and SVF). When LOW, the ancillary timing reference data is ignored.

Control Register Definitions (continued)

Ancillary Data ID Register (07)

Reg	Bit	Name	Description
07	7-0	ANCID	Bits 7-1 determine the ancillary data identification. Bit 0 is an odd parity bit, but the TMC22090 does not check parity. The value in this register must match that of the incoming ancillary data.

Subcarrier Frequency Registers

Reg	Bit	Name	Description
08	7-0	FREQ3	Eight MSBs (bits 31-24) of the 32-bit subcarrier frequency value.
09	7-0	FREQ2	Bits 23-16 of the 32-bit subcarrier frequency value.
0A	7-0	FREQ1	Bits 15-8 of the 32-bit subcarrier frequency value.
0B	7-0	FREQ0	Eight LSBs (bits 7-0) of the 32-bit subcarrier frequency value.

Subcarrier Phase Offset Registers

Reg	Bit	Name	Description
0C	7-0	SCHPHM	Eight MSBs (bits 15-8) of the 16-bit subcarrier phase offset value. Values other than 00h may be used to adjust the SCH phase of the TMC22290.
0D	7-0	SCHPHL	Eight LSBs (bits 7-0) of the 16-bit subcarrier phase offset value. Values other than 00h may be used to adjust the SCH phase of the TMC22290.

General Purpose Port Register (0E)

7	6	5	4	3	2	1	0
PORT7	PORT6	PORT5	PORT4	PORT3	PORT2	BURSTF	CSYNC

Reg	Bit	Name	Description
0E	7-6	PORT7-6	$D_{7\text{-}6}$ input pins. When in serial control mode, these register read-only bits indicate the state present on data port pins D_7 and D_6.
0E	5-2	PORT5-2	$D_{5\text{-}2}$ output pins. When in serial control mode or when reading register 0E in parallel control mode, these register read/write bits drive data pins D_5-D_2 to the state contained in the respective register bits.
0E	1	BURSTF	D_1 output pin. Produces Burst Flag when in serial control mode, or when reading register 0E.
0E	0	CSYNC	D_0 output pin. Produces Composite Sync when in serial control mode, or when reading register 0E.

Reserved Registers

Reg	Bit	Name	Description
0F-FF	7-0		Reserved. May be left unwritten.

General Purpose Port

The TMC22290 provides a general purpose I/O port for system utility functions. Input, output, and sync functions are implemented. Register 0E is the General Purpose Register.

Full functionality is provided when the encoder is in Serial control mode ($\overline{SER}$ = LOW). Most of the functions are available in parallel interface mode ($\overline{SER}$ = HIGH).

General Purpose Input (serial mode only)

Bits 7 and 6 of Register 0E are general purpose inputs. When the encoder is in serial control mode, data bits D_7 and D_6 are connected to these register locations. When Register 0E is read, the states of bits 7 and 6 reflect the TTL levels present on D_7 and D_6, respectively, at the time of read command execution. Writing to these bits has no effect.

This function is not available when the encoder is in parallel control mode.

General Purpose Output

Register 0E read/write bits 5-2 are connected to pins $D_{5\text{-}2}$, respectively, when the encoder is in serial control mode. The output pins continually reflects the values most recently written into register 0E (1 = HIGH, 0 = LOW). Note that these pins are always driven outputs when the encoder is in serial control mode.

When register 0E is read, these pins report the values previously stored in the corresponding register bits, i.e., it acts as a read/write register. When the encoder is in parallel control mode, this reading produces the output bit values on the corresponding data pins, just as in the serial control mode. However, the values are only present when reading register 0E. The controller can command a continuous read on this register to produce continuous outputs from these pins.

Burst Flag and Composite Sync (output/ read-only)

Register 0E bit 1 is associated with the encoder burst flag. It is a 1 (HIGH) from just before the start of the colorburst to just after the end of the burst. It is a 0 (LOW) at all other times. It is internally delayed to match the internal encoder latency, and is synchronous with the LUMA and COMPOSITE D/A outputs.

Register 0E bit 0 reports the encoder composite sync. It is a 0 (LOW) during horizontal and vertical sync tips. It is a 1 (HIGH) at all other times.

These register bits may be read at any time over either the serial or parallel control port. As they are dynamic, their states will change as appropriate during a parallel port read. In fact, if the parallel control port is commanded to read register 0E continually, the pins associated with these bits behave as burst flag and composite sync timing outputs.

In serial control mode, these same data output pins ($D_{1\text{-}0}$) always act as a burst flag and composite sync TTL outputs, the conditions of the serial control notwithstanding. The states of the flags may be read over the serial port, but due to the low frequency of the serial interface, it may be difficult to get meaningful information.

Horizontal and Vertical Timing

Horizontal and vertical video timing in the TMC22290 is preprogrammed for line-locked systems with a 2x pixel clock of 27.0 MHz.

Table 5 and Table 6 show timing parameters for NTSC and PAL standards as well as the actual expected timing for the TMC22290. Exactly 712 pixels of active video are provided by the user for 525/60 standards, 708 pixels for 625/50 systems. The TMC22290 precisely controls the duration and activity of all other segments of the horizontal line and vertical field group.

The vertical field group comprises several different line types based upon the Horizontal line time.

H = (2 x SL) + (2 x SH) [Vertical sync pulses]

= (2 x EL) + (2 x EH) [Equalization pulses]

SMPTE 170M NTSC and Report 624 PAL video standards call for specific rise and fall times on critical portions of the video waveform. The chip does this automatically, requiring no user intervention. The TMC22290 digitally defines slopes compatible with SMPTE 170M NTSC or CCIR Report 624 PAL on all vital edges:

1. Sync leading and trailing edges.
2. Burst envelope.
3. Active video leading and trailing edges.
4. All vertical interval equalization pulse and sync edges.

Table 5. Horizontal Timing Standards and Actual Values for 60 fps Video Standards (μs)

Parameter		NTSC (SMPTE 170M)			PAL-M (CCIR 624)			TMC22290
		Min	Nom	Max	Min	Nom	Max	
Front porch	FP	1.4	1.5	1.6	1.27		2.22	1.48
Horiz. Sync	SY	4.6	4.7	4.8	4.6	4.7	4.8	4.74
Breezeway	BR	0.508	0.608	0.809	0.9	1.1	1.3	0.59 (NTSC) 1.04 (PAL-M)
Color Burst	BU	2.235	2.514	2.794	2.237	2.517	2.797	2.37
Color Back porch	CBP	0.998	1.378	1.857	0.503		2.363	1.63 (NTSC) 1.19 (PAL-M)
Blanking	BL	10.5	10.7	11.0	10.7	10.9	11.1	10.81
Active Video	VA	52.56	52.86	53.06	52.46	52.66	52.86	52.74
Line Time	H		63.556			63.556		63.56
Equalization HIGH	EH		29.5			29.5		29.41
Equalization LOW	EL		2.3			2.3		2.37
Sync HIGH	SH		4.7			4.7		4.74
Sync LOW	SL		27.1			27.1		27.04
Sync rise and fall times			140±20 ns			<250 ns		150

Table 6. Horizontal Timing Standards and Actual Values for 50 fps Video Standards (μs)

Parameter		PAL-B,G,H,I (CCIR 624)			PAL-N (CCIR 624)			TMC22290
		Min	Nom	Max	Min	Nom	Max	
Front porch	FP	1.2	1.5	1.8	1.2	1.5	1.8	1.41
Horiz. Sync	SY	4.5	4.7	4.9	4.5	4.7	4.9	4.74
Breezeway	BR	0.6	0.9	1.2	0.6	0.9	1.2	0.89
Color Burst	BU	2.030	2.255	2.481	2.233	2.513	2.792	2.37
Color Back porch	CBP		2.654			2.387		2.15
Blanking	BL	11.7	12.0	12.3	11.7	12.0	12.3	11.56
Active Video	VA	51.7	52.0	52.3	51.7	52.0	52.3	52.44
Line Time	H		64			64		64.0
Equalization HIGH	EH		29.65			29.65		29.63
Equalization LOW	EL		2.35			2.35		2.37
Sync HIGH	SH		4.7			4.7		4.74
Sync LOW	SL		27.3			27.3		27.26
Sync rise and fall times			250±50 ns			200±100 ns		240

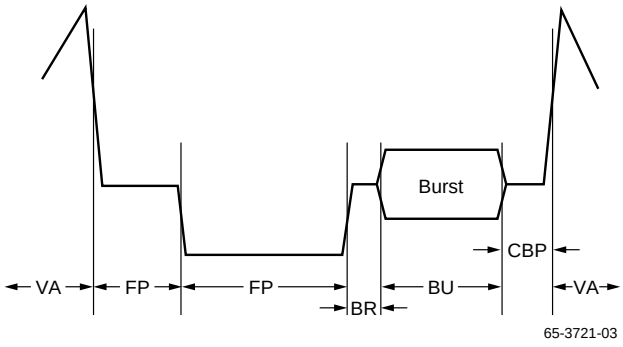


Figure 3. Horizontal Blanking Interval Timing

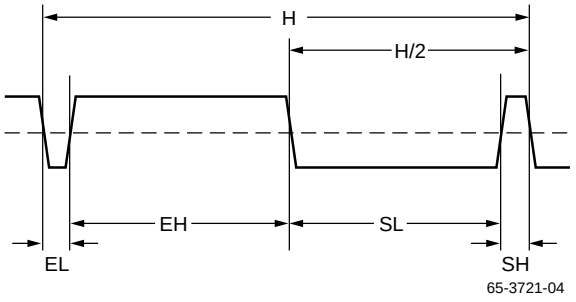


Figure 4. Vertical Sync and Equalization Pulse Detail

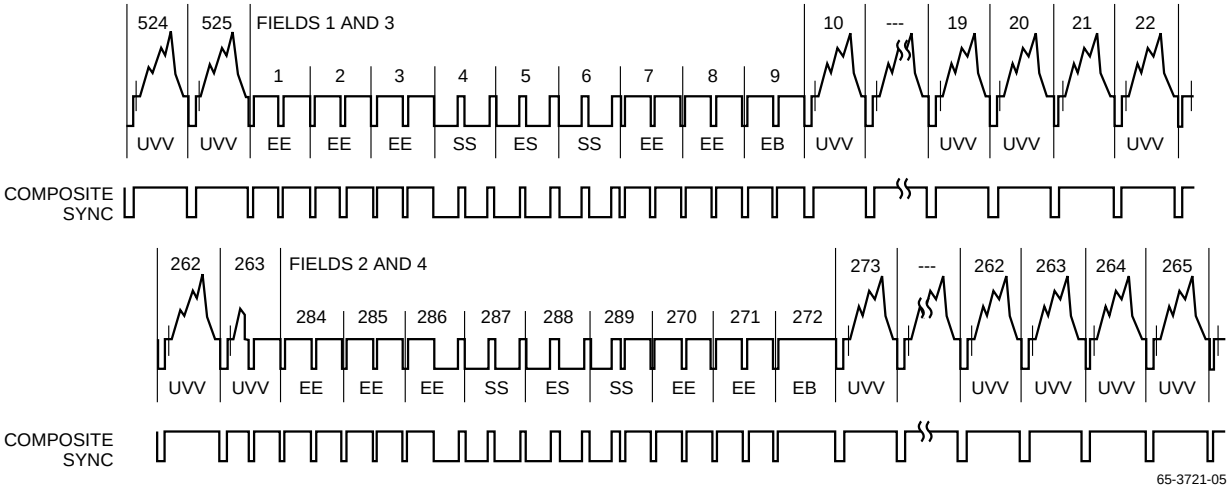


Figure 5. NTSC Vertical Interval

Table 7. NTSC Field/Line Sequence and Identification

Field 1 FID = 00		Field 2 FID = 01		Field 3 FID = 10		Field 4 FID = 11	
Line	**ID**	**Line**	**ID**	**Line**	**ID**	**Line**	**ID**
1	EE	264	EE	1	EE	264	EE
2	EE	265	EE	2	EE	265	EE
3	EE	266	ES	3	EE	266	ES
4	SS	267	SS	4	SS	267	SS
5	SS	268	SS	5	SS	268	SS
6	SS	269	SE	6	SS	269	SE
7	EE	270	EE	7	EE	270	EE
8	EE	271	EE	8	EE	271	EE
9	EE	272	EB	9	EE	272	EB
10	UVV	273	UVV	10	UVV	273	UVV
•••	•••	•••	•••	•••	•••	•••	•••
262	UVV	524	UVV	262	UVV	524	UVV
263	UVE	525	UVV	263	UVE	525	UVV

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
UVE Half-line video, half-line equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UVV Active video

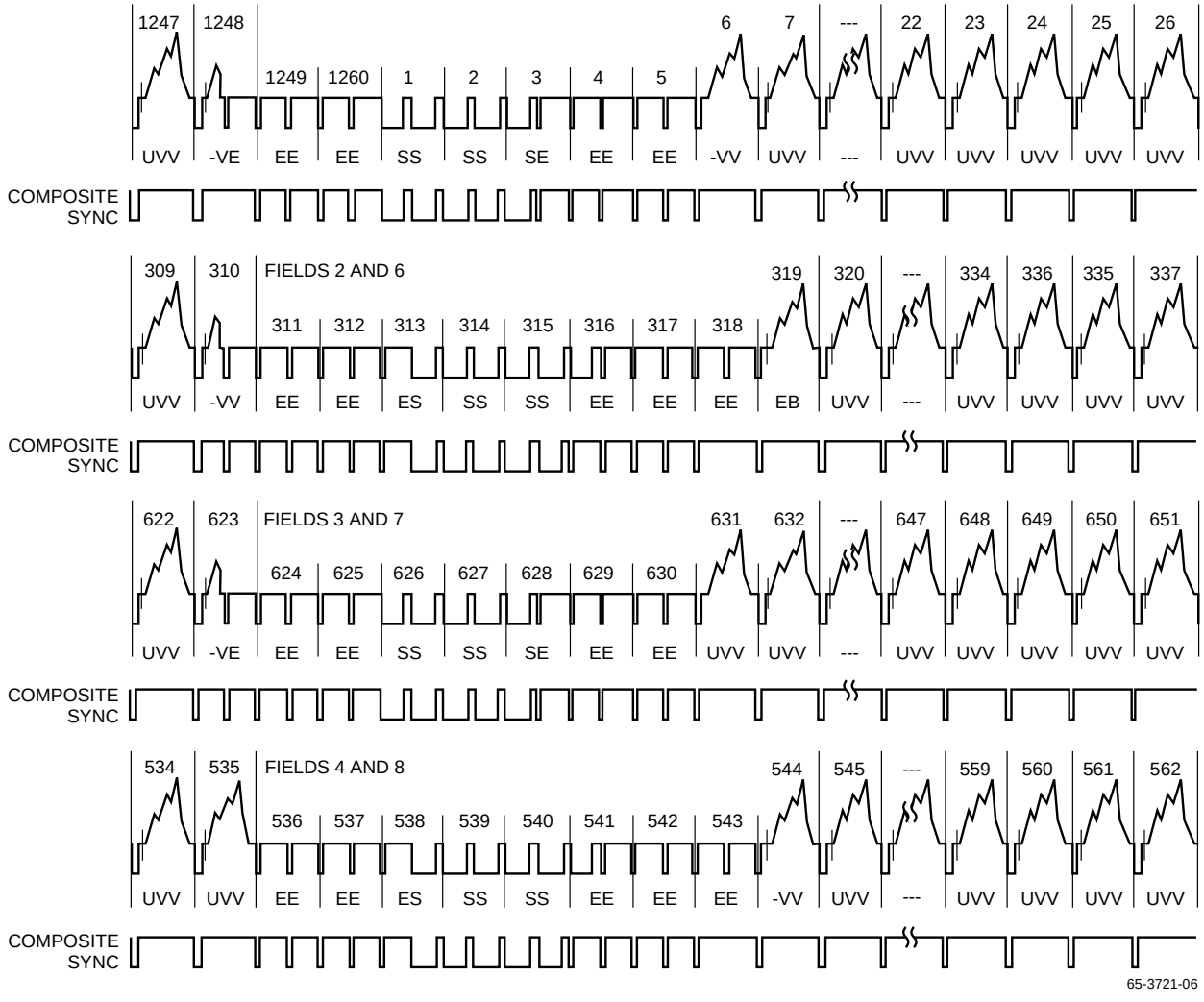


Figure 6. PAL-B, G, H, I, N Vertical Interval

Table 8. PAL-B, G, H, I, N Field/Line Sequence and Identification

Fields 1 and 5 FID = 000, 100		Fields 2 and 6 FID = 001, 101		Fields 4 and 8 FID = 011, 111		Fields 4 and 8 FID = 011, 111	
Line	**ID**	**Line**	**ID**	**Line**	**ID**	**Line**	**ID**
1	SS	313	ES	626	SS	938	ES
2	SS	314	SS	627	SS	939	SS
3	SE	315	SS	628	SE	940	SS
4	EE	316	EE	629	EE	941	EE
5	EE	317	EE	630	EE	942	EE
6	-VV	318	EV	631	UVV	943	EB
7	UVV	319	UVV	632	UVV	944	-VV
8	UVV	320	UVV	633	UVV	945	UVV
•••	•••	•••	•••	•••	•••	•••	•••
308	UVV	621	UVV	933	UVV	1246	UVV
309	UVV	622	-VV	934	UVV	1247	UVV
310	-VV	623	-VE	935	UVV	1248	-VE
311	EE	624	EE	936	EE	1249	EE
312	EE	625	EE	937	EE	1250	EE

EE Equalization pulse
SE Half-line vertical sync pulse, half-line equalization pulse
SS Vertical sync pulse
ES Half-line equalization pulse, half-line vertical sync pulse
EB Equalization broad pulse
UVV Active video
-VV Active video with color burst suppressed
-VE Half-line video, half-line equalization pulse, color burst suppressed

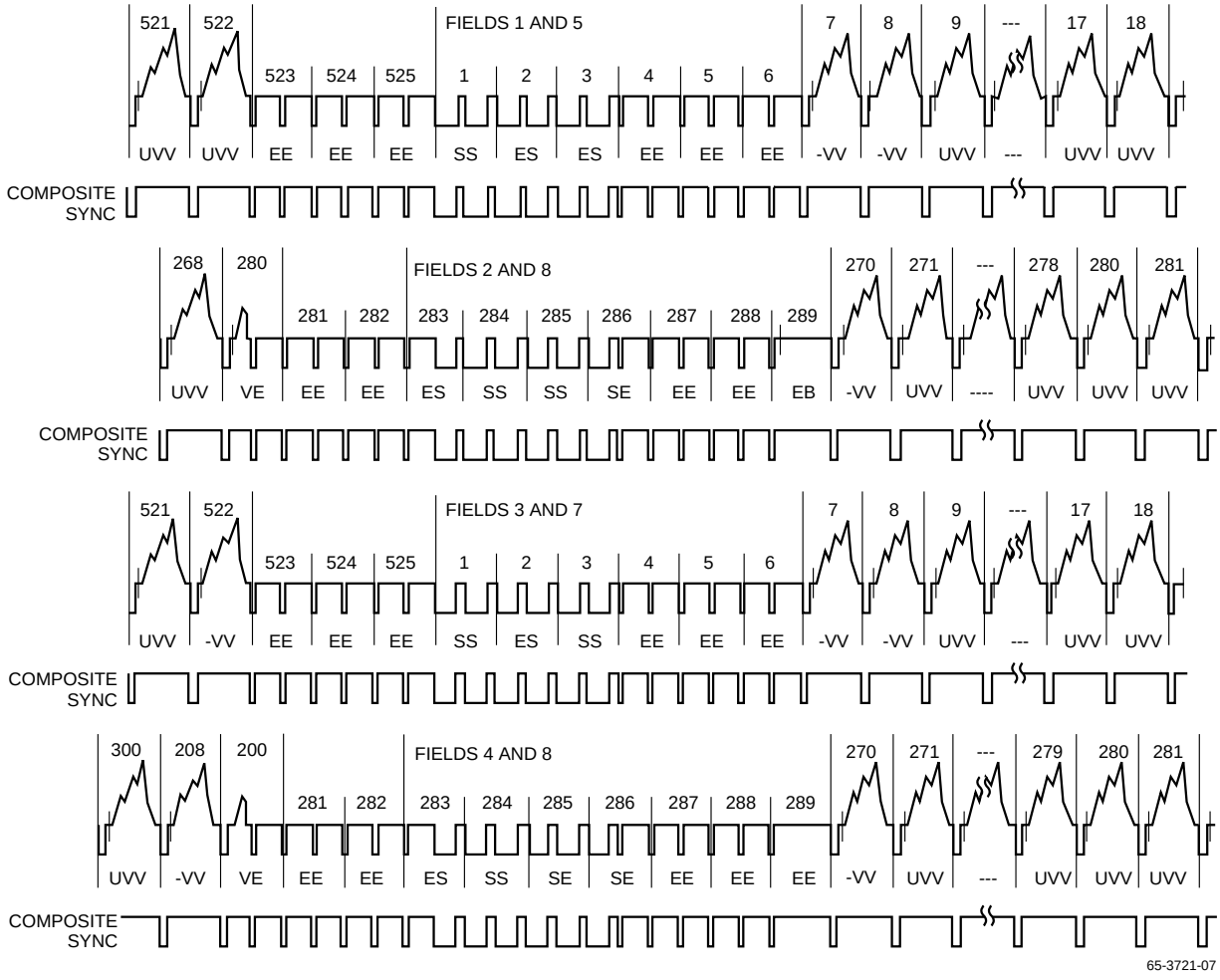


Figure 7. PAL-M Vertical Interval

Table 9. PAL-M Field/Line Sequence and Identification

Field 1 and 5 FID = 000, 100		Field 2 and 6 FID = 001, 101		Field 3 and 7 FID = 010, 110		Field 4 and 8 FID = 011, 111	
Line	**ID**	**Line**	**ID**	**Line**	**ID**	**Line**	**ID**
1	SS	263	ES	1	SS	263	ES
2	SS	264	SS	2	SS	264	SS
3	SS	265	SS	3	SS	265	SS
4	EE	266	SE	4	EE	266	SE
5	EE	267	EE	5	EE	267	EE
6	EE	268	EE	6	EE	268	EE
7	-VV	269	EB	7	-VV	269	EB
8	-VV	270	-VV	8	UVV	270	-VV
9	UVV	271	UVV	9	UVV	271	UVV
•••	•••	•••	•••	•••	•••	•••	•••
258	UVV	521	UVV	258	UVV	521	UVV
259	UVV	522	-VV	259	-VV	522	UVV
260	-VE	523	EE	260	-VE	523	EE
261	EE	524	EE	261	EE	524	EE
262	EE	525	EE	262	EE	525	EE

EE Equalization pulse
SS Vertical sync pulse
EB Equalization broad pulse
SE Half-line vertical sync pulse, half-line equalization pulse
ES Half-line equalization pulse, half-line vertical sync pulse
UVV Active video
-VV Active video with color burst suppressed
-VE Half-line video, half-line equalization pulse, color burst suppressed
UVV half-line black, half-line video

Subcarrier Generation and Synchronization

The color subcarrier is produced by an internal digital frequency synthesizer with programmable frequency and phase. The subcarrier synthesizer gets its frequency and phase values from the control registers or ancillary data packet.

The subcarrier is internally synchronized to establish and maintain a specific relationship between the leading edge of horizontal sync and color burst phase (SCH). In NTSC and PAL, SCH synchronization is performed every eight fields, on field 1 of the eight-field sequence. Proper subcarrier phase is maintained through the entire eight field set, including the 25 Hz offset in PAL-N,B,I systems

The subcarrier synthesizer seed value (stored in FREQ3, FREQ2, FREQ1, and FREQ0) depends upon the desired subcarrier frequency and the pixel rate:

$$FREQ_{10} = (\text{Subcarrier frequency} / 13.5\ \text{MHz}) \times 2^{32}$$
$$= (\text{Subcarrier cycles per line} / \text{pixels per line}) \times 2^{32}$$

Converting $FREQ_{10}$ to hexadecimal yields the values for the FREQ3, FREQ2, FREQ1, and FREQ0 registers.

SCH Phase Error Correction

SCH refers to the timing relationship between the 50% point of the leading edge of horizontal sync and the positive or negative zero-crossing of the color burst subcarrier reference. In PAL, SCH is defined for line 1 of field 1, but since there is no color burst on line 1, SCH is usually measured at line 7 of field 1. The need to specify SCH relative to a particular line in PAL is due to the 25 Hz offset of PAL subcarrier frequency. Since NTSC has no such 25 Hz offset, SCH applies to all lines.

Based upon the operating mode of the TMC22290, the subcarrier phase may be reset once every eight fields, on a line-by-line basis, or not at all (free run). The resetting of subcarrier phase is always synchronized with the 50% point of the falling edge of horizontal sync. When eight field reset is employed, the subcarrier is reset to the phase values found in Table 10.

Table 10. Subcarrier and Color Burst Reset Values

	NTSC	PAL-M	PAL-B,G,H,I,N
Digital field: Line number:	1 4	1 4	1 1
Subcarrier phase reset value:	180°	0°	0°
Resultant color burst phase:	0°	+135°	+135°

Note: Line numbering is in accordance with Figure 5, Figure 6, and Figure 7. Subcarrier and color burst phase are relative to the horizontal reference of the line specified above.

The SCHPH control register are used to compensate subcarrier phase for any group delay variation in external analog filters. This register adds a constant phase shift to the subcarrier. This phase offset is adjustable from 0° to 360° . An SCHPH value of 0000h equals 0° offset while an SCHPH value of 8000h is equal to 180°.

A 13-bit subcarrier phase value from the ancillary data packet will set the absolute phase of the subcarrier synthesizer on a line-by-line basis. If the phase values from the ancillary data are not used, the absolute phase of the synthesizer is set to zero. The SCHPH phase value is a phase offset added to subcarrier phase after the synthesizer.

Table 11. Standard Subcarrier Parameters

Standard	Horizontal Frequency (MHz)	Subcarrier Frequency (MHz)	FREQ Registers (hex)	PHASE Register (hex)	SCHPH Register (hex)
NTSC	15.734266	3.579545455	43E0F83E	0000	0000
PAL B,G,H,I	15.625000	4.43361875	54131596	0000	0000
PAL-M	15.734266	3.57561189	43CDDFC7	0000	0000
PAL-N	15.625000	3.58205625	43ED288D	0000	0000

Note: The PHASE Register is accessed via the ancillary data packet only.

Luminance Processing

During horizontal and vertical blanking, the luma processor generates blanking levels and properly timed and shaped sync and equalization pulses. During active video, it captures and rescales the incoming Y components and adds the results to the blank level to complete a proper monochrome television waveform, which is then upsampled 2:1 to drive the luma DAC and the composite adder.

For NTSC-EIA (5:2 white:sync, no black pedestal), the overall luma input-to-output transfer function for 0<Y<255 is:

luma out (IRE, relative to blank) =
(Y - 16) * 100/219

For NTSC and PAL-M (5:2, with 7.5 IRE pedestal), the equation becomes:

luma out (IRE, relative to blank) =
(Y - 16) * 92.5/219 + 7.5

For all common 625-line PAL standards (7:3, no pedestal), the equation becomes:

luma out (mV, relative to blank) =
(Y-16) * 700/219

Since Y=0 and Y=255 are reserved values in CCIR-601, a trap causes them to output black, i.e., 0mV or 0 IRE without pedestal, 7.5 IRE with pedestal.

Table 12. Luminance Input Codes

PD_{7-0} Input		Luma Level	NTSC, PAL-M Luma Level (IRE)		PAL-B, G, H, I, N Luma Level
Dec	Hex	(CCIR-601)	PEDEN = 0	PEDEN = 1	(mV)
255	FF	reserved	0	7.5	0
254	FE		108.7	108	761
235	EB	100% white	100	100	700
16	10	Black	0	7.5	0
1	01		-6.9	1.2	-48
0	00	reserved	0	7.5	0

Table 13. D/A Converter and Analog Levels

Video Level	NTSC, PAL-M		NTSC w/o Setup		PAL-B, G, H, I, N	
	D/A	IRE	D/A	IRE	D/A	mV
Maximum Output	511	137.2	511	137.2	511	977.5
100% white	405	100	405	100	400	700
Black	141	7.37	120	0	120	0
Blank	120	0	120	0	120	0
Sync	6	40	6	-40	0	-300
White-to-blank	285	100	285	100	280	700
White-to- sync	399	140	399	140	400	1000
Color burst	114	40	114	-40	120	300

Filtering Within the TMC22290

The TMC22290 incorporates internal digital filters to establish appropriate bandwidths and simplify external analog filter designs.

The chroma portion of the incoming digital video is band-limited to reduce edge effect and other distortions of the image compression process. Chrominance bandwidth is selected by CHRBW (control register 05, bit 5). When LOW, the chrominance passband attenuation is <3 dB ±650 kHz from f_{SC}. The stopband rejection is >20 dB outside f_{SC} ±2 MHz. When HIGH, the chrominance passband attenuation is <3 dB ±1.3 MHz from f_{SC}. The stopband rejection is >20 dB outside f_{SC} ±4 MHz.

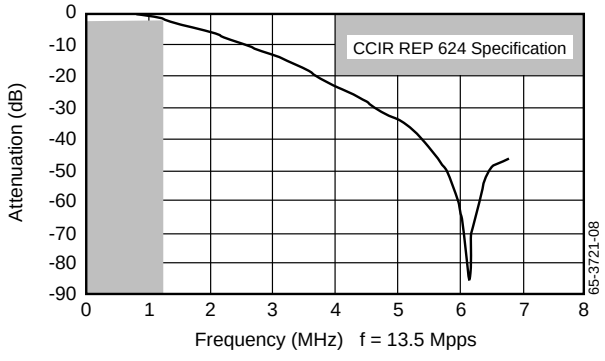


Figure 8. Color-Difference Low-Pass Filter Response

The Chroma Modulator output and the luminance data path are digitally filtered with sharp-cutoff low-pass interpolation filters. These filters ensure that aliased subcarrier, chrominance, and luminance frequencies are sufficiently suppressed in the frequency band above base-band video and below the pixel frequency ($f_S/4$ to 3 x $f_S/4$, where f_S is the PXCK frequency).

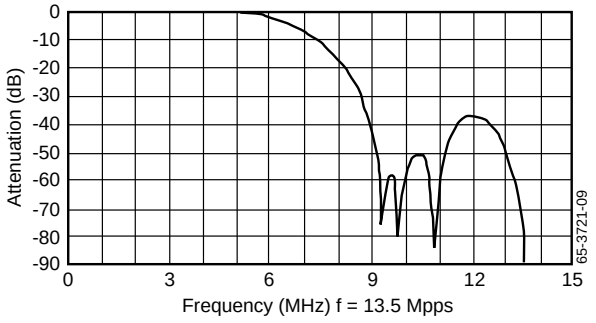


Figure 9. Chrominance and Luminance Interpolation Filter - Full Spectrum Response

Virtually all digital-to-analog reconstruction systems exhibit a high frequency roll-off as a result of the zero-order hold characteristic of classic D/A converters. This response is commonly referred to as a sin(x)/x response. It is a function of the sampling rate of the output D/A.

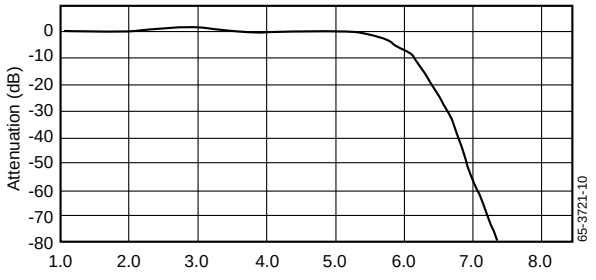


Figure 10. Chrominance and Luminance Interpolation Filter - Passband Detail

The TMC22290's digital interpolation filters convert the data stream to a sample rate of twice the pixel rate. This results in much less high frequency sin(x)/x rolloff and the output spectrum between $f_S/4$ and 3 x $f_S/4$ contains very little energy. Since there is so little signal energy in this frequency band, the demands placed on the output reconstruction filter

are greatly reduced. The output filter needs to be flat to $f_S/4$ and have good rejection at 3 x $f_S/4$. The relaxed requirements greatly simplify the design of a filter with good phase response and low group delay distortion. A small amount of peaking may be used to compensate residual sin(x)/x rolloff.

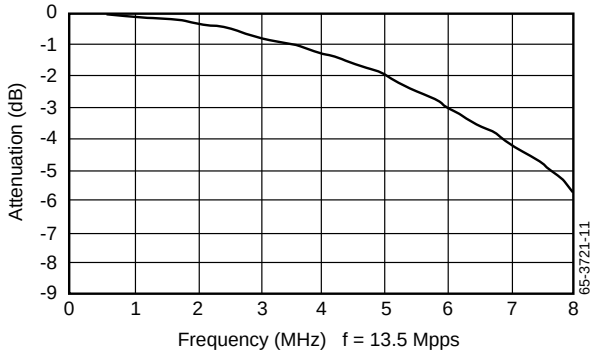


Figure 11. Sin(x)/x Response At 1x Pixel-Rate Conversion

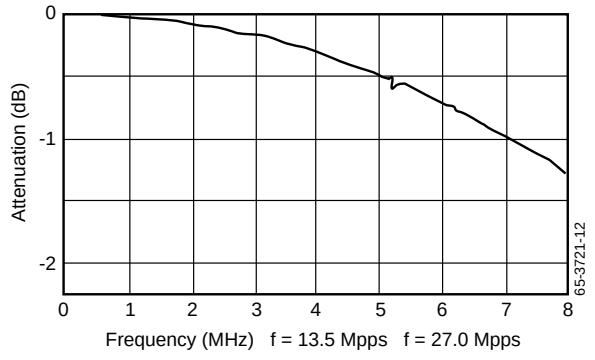


Figure 12. Sin(x)/x Response At 2X Pixel-Rate Conversion

Ancillary Data

The TMC22290 is designed to accept 15 words of ancillary data after the active video pixels at the end of each horizontal line. Ancillary data may occur once per line, once per field, once per eight fields, on random lines, or not al all. The TMC22290 does not assume ancillary data is present on a regular basis.

The first three words of ancillary data comprise the TRS signal (ANC2-0) which indicates the end of active video. Also known as the Ancillary Data Header, the TRS signal is a 00_h, FF_h, FF_h sequence. Except for the TRS words, ancillary data bit 0 (B_0, LSB) is odd parity for B_{7-1}.

The data type word (TT) is used to specify the ancillary data type. The TMC22290 compare this 7-bit value with the contents of the ANCID control register. If there is a match, the ancillary data will be processed. If there is no match, the TMC22290 ignores ancillary data.

The word count data (D_{11-0} in MM, LL) in the ancillary data packet is ignored. Ancillary data that matches the programmed Data Type is assumed to be 9 bytes long.

Ancillary phase data is used to program the MSBs of the PHASE register. ANCPHEN and PHV determine how ancillary phase data is used. When ancillary data is not present, the TMC22290 assumes PHV = LOW.

Table 14. ANCPHEN and PHV function

ANCPHEN	PHV	Description
0	x	Ignore ancillary phase data, set PHASE = 0
1	0	Ignore ancillary phase data, no change to PHASE
1	1	Load ancillary phase data into PHASE registers

Ancillary frequency data is used to program the 32-bits of the FREQ3-0 registers. ANCFREN and FRV determine how ancillary frequency data is used. When ancillary data is not present, the TMC22290 assumes FRV = LOW.

Table 15. ANCFREN and FRV function

ANCFREN	FRV	Description
0	x	Ignore ancillary frequency data
1	0	Ignore ancillary frequency data
1	1	Load ancillary frequency data into FREQ3-0 registers

Table 16. Ancillary Data Sequence

Word ID	Description	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
ANC2	Ancillary Data Header	0	0	0	0	0	0	0	0
ANC1	(Timing Reference	1	1	1	1	1	1	1	1
ANC0	Signal)	1	1	1	1	1	1	1	1
TT	Data Type	TT6	TT5	TT4	TT3	TT2	TT1	TT0	P
MM	Word	0	X	X	X	X	X	X	P
LL	Count	0	X	X	X	X	X	X	P
FIELD	Field ID / Synchronous Video Flag	x	x	x	$\overline{SVF}$	F2	F1	F0	P
	reserved	x	x	x	x	x	x	x	P
PH1	Subcarrier	PHV	PH_{12}	PH_{11}	PH_{10}	PH_9	PH_8	PH_7	P
PH0	Phase	PH_6	PH_5	PH_4	PH_3	PH_2	PH_1	PH_0	P
FR4		FRV	x	x	FR31	FR30	FR29	FR28	P
FR3	Subcarrier	FR_{27}	FR_{26}	FR_{25}	FR_{24}	FR_{23}	FR_{22}	FR_{21}	P
FR2		FR_{20}	FR_{19}	FR_{18}	FR_{17}	FR_{16}	FR_{15}	FR_{14}	P
FR1	Frequency	FR_{13}	FR_{12}	FR_{11}	FR_{10}	FR_9	FR_8	FR_7	P
FR0		FR_6	FR_5	FR_4	FR_3	FR_2	FR_1	FR_0	P

P = odd parity bit, x = reserved bit - set to 0

Table 17. Field Identification and Subcarrier Reset Modes

ANCTREN	$\overline{SVF}$	F_2	F_1	F_0	F (EAV)	Field ID / Subcarrier Reset Mode
Basic Mode						
0	x	x	x	x	0	odd field, reset subcarrier every 8 fields
0	x	x	x	x	1	even field
Genlocking Mode						
1	1	x	x	x	0	odd field, subcarrier free run
1	1	x	x	x	1	even field
Field Sequence Mode						
1	0	0	0	0	X	Field 1, reset subcarrier at field 1
1	0	0	0	1	X	Field 2
1	0	0	1	0	X	Field 3
1	0	0	1	1	X	Field 4
1	0	1	0	0	X	Field 5
1	0	1	0	1	X	Field 6
1	0	1	1	0	X	Field 7
1	0	1	1	1	X	Field 8

The F bit is part of the EAV timing reference code and tracks the F0 bit

Operating Modes

The field number bits (F_{2-0}) from the ancillary data packet FIELD word, are used to program the encoder's field counter depending upon the state of the synchronous video flag ($\overline{SVF}$) and the ANCTREN bit in the control register.

In the basic operating mode (ANCTREN = LOW), all timing is found in the F bit of EAV. F_{2-0} and $\overline{SVF}$ are ignored and the encoder subcarrier synthesizer is reset to the PHASE value every eight fields (when the field counter transitions from 111(field 8) to 000 (field 1).

In the basic mode, ANCFREN and ANCPHEN are typically set LOW, ignoring ancillary frequency and phase data. If ANCFREN and ANCPHEN are HIGH, the TMC22290 uses the incoming ancillary frequency and phase data on a line-by-line basis.

In genlocking mode (ANCTREN and $\overline{SVF}$ = HIGH), the subcarrier synthesizer is allowed to free run, with phase and frequency being set from the ancillary data packet PH_{12-0} and FR_{31-0} data. The field counter increments just like it does in basic mode.

Field sequence mode (ANCTREN = HIGH and $\overline{SVF}$=LOW), is the same as basic mode except that the field counter is set by the F_{2-0} bits in the FIELD word of ancillary data. If ancillary data is not present on a line, the field counter will continue to count as it does in basic mode. When ancillary data is present, the contents of the field counter are loaded with field data (F_{2-0}). In this way, the TMC22290 may be synchronized with an external source by sending field data only once.

Parallel Microprocessor Interface

The parallel microprocessor interface, active when $\overline{SER}$ is HIGH, employs an 14-line interface, with an 8-bit data bus and one address bit: two addresses are required for device programming and pointer-register management. Address bit 0 selects between reading/writing the register addresses and reading/writing register data. When writing, the address is presented along with a LOW on the $\overline{R/W}$ pin during the falling edge of $\overline{CS}$. Eight bits of data are presented on D_{7-0} during the subsequent rising edge of $\overline{CS}$. One additional falling edge of $\overline{CS}$ is needed to move input data to its assigned working registers.

In read mode, the address is accompanied by a HIGH on the $\overline{R/W}$ pin during a falling edge of $\overline{CS}$. The data output pins go to a low-impedance state t_{DOZ} ns after $\overline{CS}$ falls. Valid data is present on D_{7-0} t_{DOM} after the falling edge of $\overline{CS}$. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

Table 18. Parallel Port Control

ADR	R/W\	Action
1	0	Load D_{7-0} into Control Register pointer.
1	1	Read Control Register pointer on D_{7-0}.
0	0	Write D_{7-0} to addressed Control Register.
0	1	Read addressed Control Register on D_{7-0}.

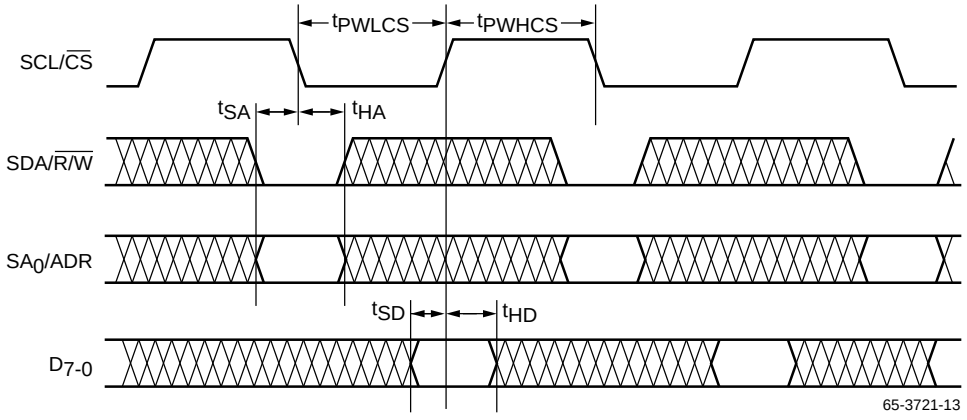


Figure 13. Microprocessor Parallel Port - Write Timing

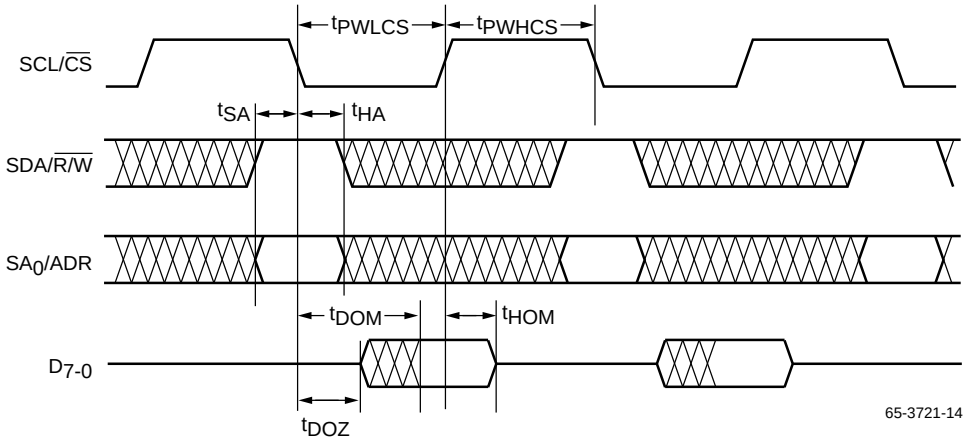


Figure 14. Microprocessor Parallel Port - Read Timing

Serial Control Port (R-Bus)

In addition to the 14-wire parallel port, a 2-wire serial control interface is also provided, and active when $\overline{SER}$ is LOW. Either port alone can control the entire chip. Up to four TMC22290 devices may be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire interface comprises a clock (SCL/$\overline{CS}$) and a bi-directional data (SDA/$\overline{R/W}$) pin. The TMC22290 acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL/$\overline{CS}$ and SDA/$\overline{R/W}$ are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA/$\overline{R/W}$ line must be stable for the duration of the positive-going SCL/$\overline{CS}$ pulse. Data on SDA/$\overline{R/W}$ must change only when SCL/$\overline{CS}$ is LOW. If SDA/$\overline{R/W}$ changes state while SCL/$\overline{CS}$ is HIGH, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL/$\overline{CS}$ and SDA/$\overline{R/W}$ are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA/$\overline{R/W}$ while SCL/$\overline{CS}$ is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address and a single R/W bit. The R/W bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_0/ADR and SA_1 input pins in Table 19.), the TMC22290 acknowledges by bringing SDA/$\overline{R/W}$ LOW on the 9th SCL/$\overline{CS}$ pulse. If the addresses do not match, the TMC22290 does not acknowledge.

Table 19. Serial Port Addresses

A_6	A_5	A_4	A_3	A_2	A_1 (SA_1)	A_0 (SA_0)
0	0	0	1	1	0	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	0	1	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the TMC22290 does not acknowledge the master device during a write sequence, the SDA/$\overline{R/W}$ remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC22290 during a read sequence, the TMC22290 interprets this as “end of data.” The SDA/$\overline{R/W}$ remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the TMC22290 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 20h. Any base address higher than 20h will not produce an ACKnowledge signal. If no ACKnowledge is received from the master, the encoder will automatically stop sending data.

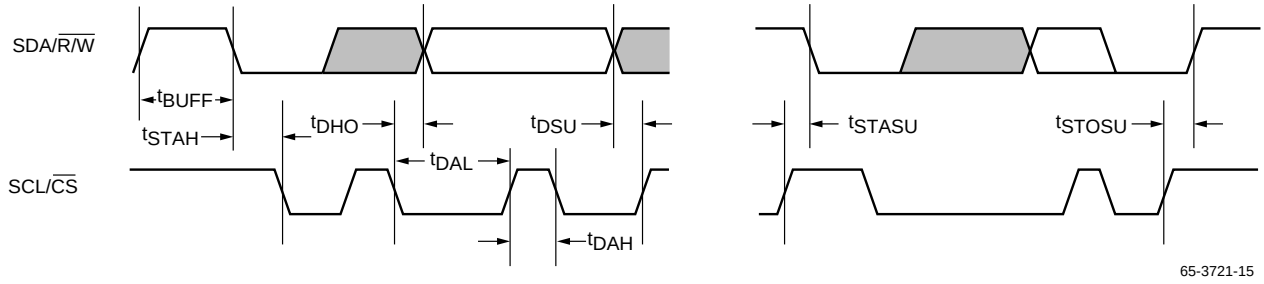


Figure 15. Serial Port Read/Write Timing

Data is read from the control registers of the TMC22290 in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the TMC22290, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA/$\overline{R/W}$ while SCL/$\overline{CS}$ is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Data byte to base address
↓ Stop signal

Write to four consecutive control registers

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Data byte to base address
↓ Data byte to (base address + 1)
↓ Data byte to (base address + 2)
↓ Data byte to (base address + 3)
↓ Stop signal

Read from one control register

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Stop signal
↓ Start signal
↓ Slave Address byte (R/W bit = HIGH)
↓ Data byte from base address
↓ Stop signal

Read from four consecutive control registers

↓ Start signal
↓ Slave Address byte (R/W bit = LOW)
↓ Base Address byte
↓ Stop signal
↓ Start signal
↓ Slave Address byte (R/W bit = HIGH)
↓ Data byte from base address
↓ Data byte from (base address + 1)
↓ Data byte from (base address + 2)
↓ Data byte from (base address + 3)
↓ Stop signal

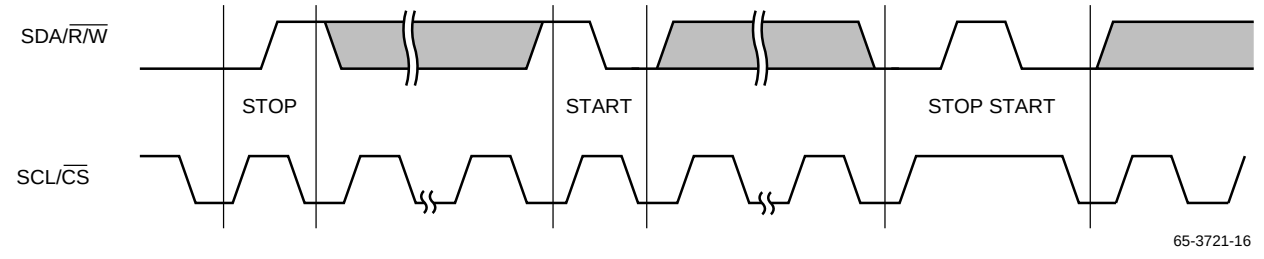


Figure 16. Serial Interface - Start/Stop Signal

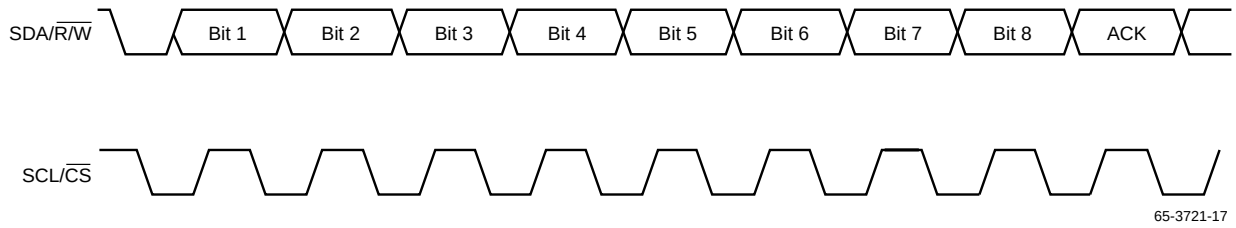


Figure 17. Serial Interface - Typical Byte Transfer

JTAG Test Interface

The JTAG test port accesses registers at every digital I/O pin except the JTAG test port pins.

Table 20 specifies the sequence of the test registers. The register number (Reg) indicates the order in which the register data is loaded and read (Reg 1 is loaded and read first, therefore it is at the end of the serial path). The scan path is 23 registers long. The six TEST pins function as JTAG registers.

The JTAG port is a 4-wire interface, following IEEE Std. 1149.1-1990 specifications. The Test Data Input (TDI) and Test Mode Select (TMS) inputs are referred to the rising edge of the Test ClocK (TCK) input. The Test Data Output (TDO) is referred to the falling edge of TCK.

The JTAG standard has been implemented into the TMC22290 without the UPDATE data register (it treats output pins and there are none on the TMC22290).

The CAPTURE Instruction Register is implemented with force value of 01 which allows SAMPLE or PRELOAD data to the data path.

The Instruction register contains two bits: IRM and IRL (TDI shift to IRM; IRM shift to IRL; IRL shift to TDO) - see Table 21.

There are 16 states in TAP and all are fully implemented.

In general, TMS is commanding the state machine and puts the system into JTAG states. The TMC22290 can be operated freely because there is no means to interrupt its function. There is NO output driver related to the JTAG data path.

While TMS determines the state, there are only a few events that may happen:

1. Capture DR. In this state, all the data at the pins will be LOADed into the data scan path only if IRM is not equal to IRL. If IRM = IRL, even though the state machine at this state, NO ACTION will take place.

2. Shift DR. In this state, the data scan path is transferring data from high order bit to low order bits. It is always operational regardless of the contents of IRM and IRL.

3. Capture IR. While TMS captures IR state, the TMC22290 automatically loads 01 to the pre-instruction register (IRMp and IRLp respectively).

4. Shift IR. In this state, shift TDI to IRMp, IRMp to IRLp, and IRLp to TDO.

5. Update IR. In this state, TMC22290 LOAD contents of the Instruction register from the PRELOADED (or SHIFTED) IR to execution Instruction register (double buffered.)

The DATA SCAN PATH Register is a serial SHIFT, parallel LOAD shift register. While in Shift DR state, TMC22290 does SHIFT. While the IR (instruction register) is 01 or 10, and the TAP state is at Capture DR state, TMC22290 does LOAD.

For each input PIN (tri-state pins included, but not the analog pins), the TMC22290 has a 2:1 multiplexer and register. One of the multiplexer inputs is the PAD and the other is the shifted data from the higher order scan path.

Table 20. JTAG Sequence

Reg	Pin	Reg	Pin	Reg	Pin
1	$\overline{\text{RESET}}$	9	PD_1	17	D_6
2	PXCK	10	PD_0	18	D_5
3	PD_7	11	SA_1	19	D_4
4	PD_6	12	SA_0\ADR	20	D_3
5	PD_5	13	SDA/$\overline{\text{R/W}}$	21	D_2
6	PD_4	14	SCL/$\overline{\text{CS}}$	22	D_1
7	PD_3	15	$\overline{\text{SER}}$	23	D_0
8	PD_2	16	D_7		

Table 21. Function of IRM and IRL

IRM	IRL	Function
0	0	EXTEST, no effect while shift at DR, data keeps on shifting.
0	1	SAMPLE / PRELOAD At capture DR state, load all input pins parallel to data scan path.
1	0	Same as SAMPLE / PRELOAD
1	1	BYPASS TDI bypass to TDO

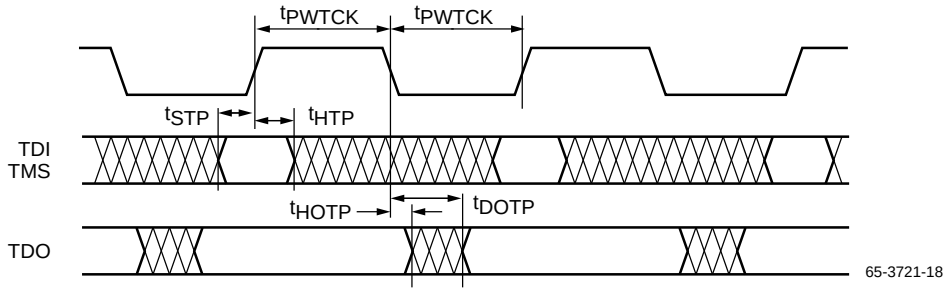


Figure 18. JTAG Test Port Timing

Equivalent Circuits

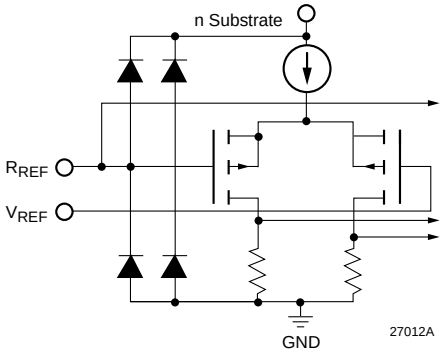


Figure 19. Equivalent Analog Input Circuit

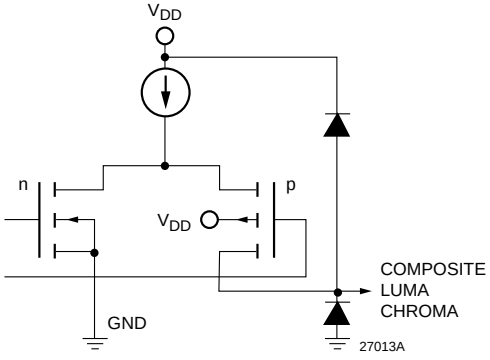


Figure 20. Equivalent Analog Output Circuit

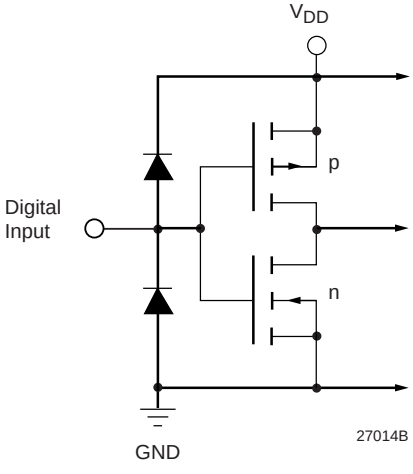


Figure 21. Equivalent Digital Input Circuit

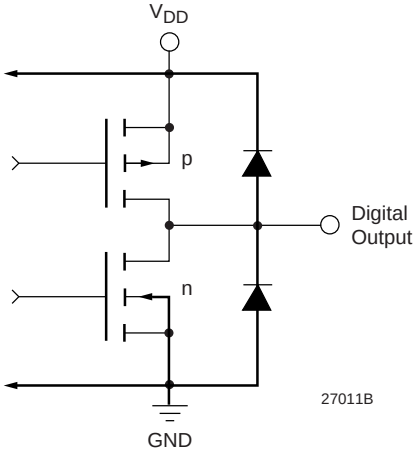


Figure 22. Equivalent Digital Output Circuit

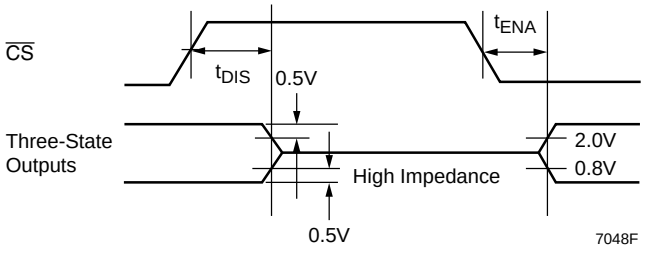


Figure 23. Threshold Levels for Three-State Measurement

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltage	-0.5		+7.0	V
Digital Inputs				
Applied Voltage	-0.5		V_{DD}+0.5	V
Forced current [3, 4]	-20.0		+20.0	mA
Output				
Applied voltage [2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-3.0		+6.0	mA
Short circuit duration (single output in HIGH state to ground)			1 second	
Analog Output Short circuit duration (all outputs to ground)			infinite	
Temperature				
Operating, ambient	-20		110	°C
junction			+140	°C
Lead, soldering (10 seconds)			+300	°C
Vapor Phase soldering (1 minute)			+220	°C
Storage	-65		+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Compatible Inputs	2.0		V_{DD}	V
	Serial Port (SDA, SCL)	.7V_{DD}			V
	CLK Input	2.4		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				V
	TTL Compatible Inputs	GND		0.8	V
	Serial Port (SDA, SCL)	GND		0.3V_{DD}	V
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current		1.57		mA
	(I_{REF}=V_{REF}/R_{REF}), flowing out of the R_{REF} pin				
R_{REF}	External Reference Resistor, V_{REF}=NOM		787		Ω
I_{OH}	Output Current, Logic HIGH (D_{7-0}, TDO)			-2.0	mA
I_{OL}	Output Current, Logic LOW (D_{7-0}, TDO)			4.0	mA
	Output Current, Logic LOW (SDA)			6.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Operating Conditions (continued)

Parameter		Min	Nom	Max	Units
Pixel Interface					
f_{PXL}	Pixel Rate		13.5		Mpps
f_{PXCK}	Master Clock Rate, = 2X pixel rate		27.0		MHz
t_{PWHPX}	PXCK pulse width, HIGH	10			ns
t_{PWLPX}	PXCK pulse width, LOW	15			ns
t_{SP}	PD_{7-0} Setup Time	10			ns
t_{HP}	PD_{7-0} Hold Time	0			ns
Parallel Microprocessor Interface					
t_{PWLCS}	CS\ Pulse Width, LOW	95			ns
t_{PWHCS}	CS\ Pulse Width, HIGH	30			ns
t_{SA}	Address Setup Time	10			ns
t_{HA}	Address Hold Time	0			ns
t_{SD}	Data Setup Time (write)	15			ns
t_{HD}	Data Hold Time (write)	8			ns
t_{SR}	Reset Setup Time	15			ns
t_{HR}	Reset Hold Time	2			ns
Serial Microprocessor Interface					
t_{DAL}	SCL Pulse Width, LOW		1.3		µs
t_{DAH}	SCL Pulse Width, HIGH		0.6		µs
t_{STAH}	SDA Start Hold Time		0.6		µs
t_{STASU}	SCL to SDA Setup Time (START)		0.6		µs
t_{STOSU}	SCL to SDA Setup Time (STOP)		0.6		ns
t_{BUFF}	SDA Stop to SDA Start Hold Time		1.3		µs
t_{DSU}	SDA to SCL Data Setup Time		300		ns
tDHO	SCL to SDA Hold Time		300		ns
JTAG Interface					
f_{TCK}	Test Clock (TCK) Rate			10	Mhz
t_{PWLTCK}	TCK Pulse Width, LOW	10			ns
t_{PWHTCK}	TCK Pulse Width, HIGH	10			ns
t_{STP}	Test Port Setup Time, TDI, TMS	10			ns
t_{HTP}	Test Port Hold Time, TDI, TMS	0			ns

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
I_{DD}	Power Supply Current[1]	V_{DD} = Max, f_{PXCK} = 27MHz			125	
I_{DDQ}	Power Supply Current, DACs disabled[2]	V_{DD} = Max, f_{PXCK} = 27MHz			75	mA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
Z_{RO}	VREF Output Impedance			1000		Ω
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = VDD			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = VDD			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	D_{7-0}, TDO, I_{OH} = MAX	2.4			V
V_{OL}	Output Voltage, LOW	D_{7-0}, TDO, I_{OL} = MAX			0.4	V
		SDA, I_{OL} = 3mA			0.4	V
		SDA, I_{OL} = 6mA			0.6	V
C_I	Digital Input Capacitance			4	10	pF
C_I	Digital Output Capacitance			10		pF
V_{OC}	Video Output Compliance		-0.3		1.6	V
R_{OUT}	Video Output Resistance			15		kΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0mA, f = 1MHz		15	25	pF

Notes:

1. Maximum I_{DD} with V_{DD} = MAX and T_A = MIN. Outputs loaded wtih 75Ω.
2. I_{DDQ} when YCDIS = COMPDIS = HIGH, disabling D/A converters.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		10			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		10			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid			30		ns
t_{DOTP}	Output Delay, TCK to TDO Valid				30	ns
t_{HOTP}	Output Hold Time, TCK to TDO Valid			5		ns
t_R	D/A Output Current Risetime	10% to 90% of full scale		2		ns
t_F	D/A Output Current Falltime	90% to 10% of full scale		2		ns
t_{DOV}	Analog Output Delay			20		ns

Note: Timing reference points are at the 50% level. Analog C_{LOAD} <10pF, D_{7-0} load <40pF.

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Units
RES	D/A Converter Resolution		9	9	9	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp		.51	1.0	degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp		.8	1.5	%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination		.1	±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination		.2	±1.0	%
CLIM	Chroma/Luma Intermodulation	NTC-7 Combination		.05		IRE
CLGI	Chroma/Luma Gain inequality	NTC-7 Composite		97.6		%
CLDI	Chroma/Luma Delay inequality	NTC-7 Composite	-5	0	5	ns
LNLD	Luma Nonlinear Distortion	NTC-7		1.0		%
FTWD	Field Time Waveform Distortion	NTC-7		.6		%
LTWD	Line Time Waveform Distortion	NTC-7		.1		%
LOTWD	Long Time Waveform Distortion, initial and peak overshoot	10% / 90% APL Bounce				IRE
LOTWD	Long Time Waveform Distortion, peak overshoot	after 5 seconds, 10% / 90% APL Bounce				IRE
LDCOFF	Line-by-Line DC Offset					IRE
DYNG	Dynamic Gain	NTC-7				IRE
NOISE	Noise Level (Note 1)	100% unmod. ramp		-65.4		dB rms
NOISE	Noise Level (Note 2)	100% unmod. ramp				dB rms
CAMN	Chroma AM Noise	Red field		-59		dB rms
CPMN	Chroma PM Noise	Red field		-59		dB rms
SYRF	Sync Pulse Rise and Fall Time					ns
BERF	Burst envelope Rise and Fall Time					ns
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 μF, f = 1 kHz		0.5		%/ %V_{DD}

Notes:

1. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode."

Applications Information

The circuit in Figure 25 shows the connection of power supply voltages, output reconstruction filters and the external voltage reference. All V_{DD} pins should be connected to the same power source.

The full-scale output voltage level, V_{OUT}, on the COMPOSITE, LUMA, and CHROMA pins is found from:

$$V_{OUT} = I_{OUT} \times RL = K \times I_{REF} \times R_L$$

$$= K \times (V_{REF}/R_{REF}) \times R_L$$

where:

1. I_{OUT} is the full-scale output current sourced by the TMC22290 D/A converters.
2. R_L is the net resistive load on the COMPOSITE, CHROMA, and LUMA output pins.
3. K is a constant for the TMC22290 D/A converters (approximately equal to 10.4).
4. I_{REF} is the reference current flowing out of the R_{REF} pin to ground.

5. V_{REF} is the voltage measured on the V_{REF} pin.

6. R_{REF} is the total resistance connected between the R_{REF} pin and ground.

The reference voltage in Figure 25 is from an LM185 1.2 Volt band-gap reference. The 392 Ohm resistor connected from R_{REF} to ground sets the overall "gain" of the three D/A converters of the TMC22290. Varying R_{REF} ±5% will cause the full-scale output voltage on COMPOSITE, LUMA, and CHROMA to vary by ±5%.

The suggested output reconstruction filter is the same one used on the TMC2063P7C Demonstration Board. The phase and frequency response of this filter is shown in Figure 24.

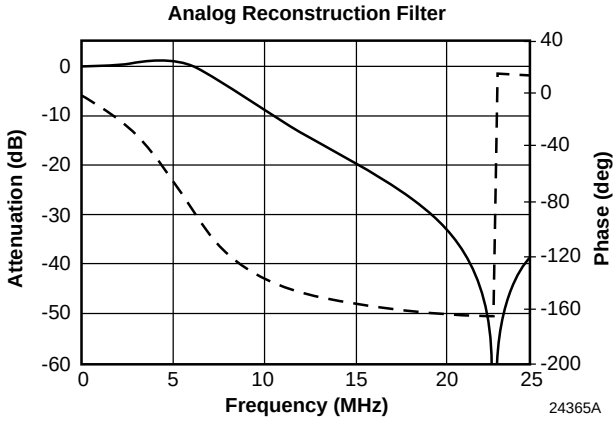


Figure 24. Response of Recommended Output Filter

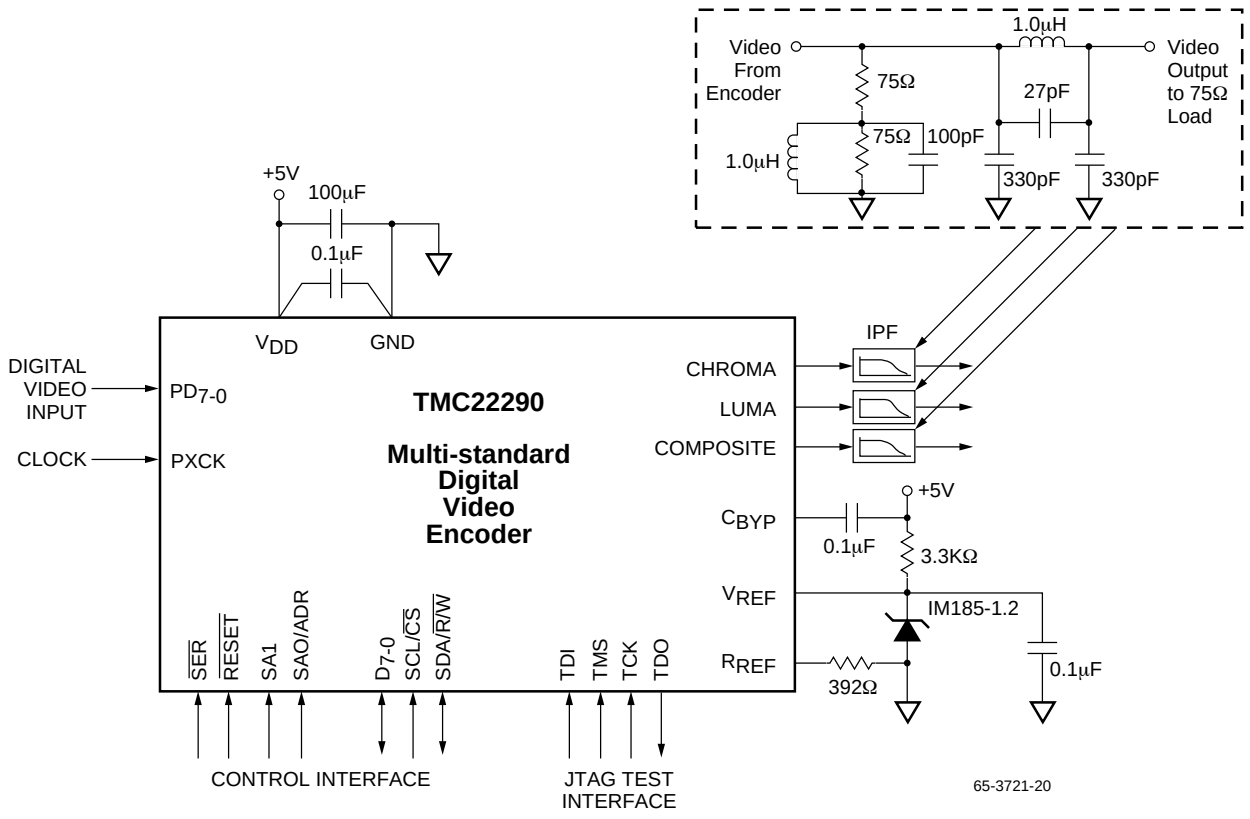


Figure 25. Typical Application Circuit

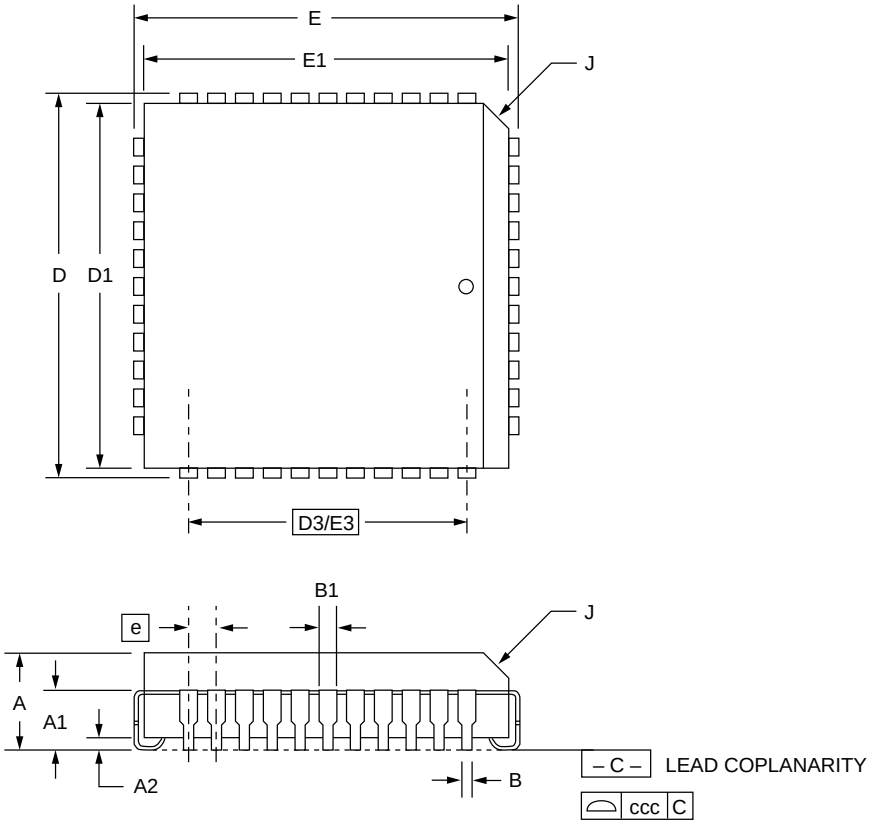
Notes:

Mechanical Dimensions – 44 Lead PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC22290R2C	0°C to 70°C	Commercial	44-Lead PLCC	22290R2C

Raytheon Electronics
Semiconductor Division
5580 Morehouse Drive
San Diego, CA 92121
619 457 1000
800 722 7074
Fax 619 455 6314
applications@lj.sd.ray.com

10/95 2.0m
Stock# DS70022290